WHAT IS CLAIMED IS:

1. A semiconductor memory receiving an external address including an array address and a row address, the memory comprising:

N memory arrays, each memory array having an array address and a plurality of normal and redundant rows of memory cells;

a redundancy block providing a match signal having an active state when the external address matches one of a plurality of defective addresses, providing a redundant row address when the match signal has the active state, and providing a redirected array address comprising a redundant array address when the match signal has the active state and otherwise comprising the external array address; and

N local row control blocks, each associated with a different one of the N memory arrays, wherein the local row control block associated with the memory array whose array address matches the redirected array address opens a redundant row of memory cells for access based on the redundant row address when the match signal has the active state and otherwise opens a normal row of memory cells for access based on the external row address.

2. The memory of claim 1, wherein the semiconductor memory comprises a random access memory.

3. The memory of claim 1, wherein the N memory arrays, the N local row control blocks, and the redundancy block together comprise a memory bank.

4. The memory of claim 3, wherein the memory bank further comprises:

a central row controller, based on the redundancy block providing the redirected array address, configured to provide a series of timing signals associated with a row operation, wherein the local row control block associated with the array whose address matches the redirected array address is configured to provide to the array a series of access signals associated with the row

operation, wherein the access signals are based on the timing signals, the redirected array address, the external row address, and the redundant row address.

5. The memory of claim 4, wherein each of the timing signals includes transitions between active and inactive states, and wherein the central row controller includes a plurality of time delay elements configured to control time delays of the timing signal transitions relative to one another such that the transitions of the timing signals occurs in a predetermined order.

6. The memory of claim 5, wherein the time delay elements are tunable such that the corresponding time delays can be adjusted.

7. The memory of claim 4, wherein the redundancy block and the central row controller together comprise a common row interface.

8. The memory of claim 5, wherein the common row interface further comprises:

a predecoder providing a predecoded row address representative of the external row address, wherein the local row control block opens a normal row of memory cells for access based on the predecoded row address.

9. The memory of claim 3, wherein the memory comprises a plurality of memory banks, each memory bank having a bank address and having a corresponding redundancy block; the memory further comprising:

a plurality of a bank controllers, each of the bank controllers associated with a different one of the plurality of memory banks and configured to receive the external address and an external bank address; wherein the bank controller associated with the memory bank whose bank address matches the external bank address is configured to provide the external address to the memory bank's associated redundancy block.

10. The memory of claim 1, wherein the redundancy block comprises:

an array redirector having the plurality of defective addresses stored therein, each having a corresponding redundant row of memory cells assigned as a replacement row and having a redundant array address and a redundant row address, the array redirector configured to compare the external address to each of the defective addresses, and when the external address matches one of the defective addresses, configured to provide the redirected array address comprising the redundant array address corresponding to the matching defective address; and

a row redirector, when a match occurs, configured to provide the redundant row address comprising the redundant row address corresponding to the matching defective address.

11. The memory device of claim 10, wherein each array has a same number of redundant rows of memory cells located at a same plurality of redundant row positions within each array, and wherein each redundant row of memory cells can be assigned as a replacement for a corresponding one of the defective addresses.

12. The memory device of claim 11, wherein each array includes four redundant rows of memory cells at a same four row positions within each array.

13. The memory of claim 11, wherein the array redirector further comprises:

N comparator blocks, each corresponding to one of the N arrays each and comprising:

a plurality of comparator circuits, each corresponding to one of the redundant row positions within the corresponding array and storing therein the defective address of a defective row of memory cells for which the corresponding redundant row position has been assigned as a replacement, and configured to compare the external address to the

defective address stored therein and to provide a row position signal having an active state when a match occurs; and

a combiner configured to provide an array match signal associated with the corresponding array having an active state when any one of the row position signals has the active state; and

N memory locations, each associated with one of the N comparator blocks and each storing the array address of the array corresponding to the associated comparator block, and configured to provide the array address stored therein as the redundant array address in response to the array match signal from the corresponding comparator block having the active state.

14. The memory of claim 13, wherein the combiner comprises an OR-gate.

15. The memory of claim 13, wherein the array redirector further comprises a combiner configured to provide the match signal having the active state when any one of the array match signals from the N comparator blocks has the active state, and is configured to provide the external array address as the redundant array address when the match signal does not have the active state.

16. The memory of claim 15, wherein the combiner comprises a wired OR-gate.

17. The memory of claim 13, wherein the row redirector further comprises:

a plurality of combiner blocks, each corresponding to a different one of the redundant row positions and configured to receive from each of the N comparator blocks the row position signal from the comparator circuit associated with the corresponding redundant row position, each combiner block configured to provide a redundant row signal having a state based on the states of the row position signals, wherein the redundant row signals from each the of the combiners together form the redundant row address.

18. The memory of claim 13, wherein each of the combiner blocks comprises a wired OR-gate.

19. A semiconductor memory receiving an external address including an array address and a row address, the memory comprising:

a memory bank having N arrays, each array having an array address and a plurality of rows of memory cells;

a central row controller, in response an activate command indicative of a bank transaction having an active state, configured to provide a series of timing signals associated with a row operation; and

N local control blocks, each associated with a different one of the N arrays, wherein the local control block associated with the array whose address matches the external array address is configured to provide to the array a series of access signals associated with row operation, wherein the access signals are based on the timing signals, the array address, and the row address.

20. The memory of claim 19, wherein the central row controllers provides each of the timing signals with transitions between active and inactive states, and wherein the central row further includes a plurality of time delay elements configured to control time delays of the timing signal transitions relative to one another such that the transitions of the timing signals occurs in a predetermined order.

21. The memory of claim 20, wherein the time delay elements are tunable such that the corresponding timing delays can be adjusted.

22. A method of operating a random access memory device including N memory arrays, each memory array having an array address and a plurality of normal and redundant rows of memory cells, the method comprising:

receiving an external address including an array address and a row address;

providing a match signal having an active state when the external address matches one a plurality of defective addresses;

providing a redundant row address when the match signal has the active state;

providing a redirected array address comprising a redundant array address when the match signal has the active state and otherwise comprising the external array address.

23. The method of claim 22, further comprising:

opening a redundant row of memory cells for access based on the redundant row address when the match signal has the active state, otherwise opening a normal row of memory cells for access based on the external row address.